

What is claimed is:

1. (Currently amended) A bipolar transistor on a substrate comprising a base (4, 12) with an inner base portion (4a) and an outer base portion (4b) which adjoins the inner base portion (4a) in a lateral direction in parallel relationship with the substrate surface and in a heightwise direction facing perpendicularly with respect to the substrate surface and is of a greater extent than the inner base portion (4a), wherein the base includes a first epitaxial base layer (4) and a second base layer (12) disposed on the first and the second base layer (12) and is opened in the lateral region of the inner base portion (4a) to form an emitter window (9, 4a),

an emitter (9) of a T-shaped cross-sectional profile, which is separated from the outer base portion (4b) laterally by a spacer (8) of insulating material and whose portion corresponding to the vertical bar of the T-shape adjoins with its lower end in the heightwise direction the inner base portion (4a),

in which beneath a portion of the emitter (9) which corresponds to the horizontal bar of the T-shape the lateral extent (d) of the spacer (8) increases from its interface with the inner base portion (4a) with increasing height over the inner base portion (4a),

wherein a first interface formed by the emitter (9) and the spacer (8) meets a second interface formed by the emitter and the inner base portion at a first angle (α) which is either a right angle or an obtuse angle, and

a third interface formed by the spacer (8) and the outer base portion (4b) meets the second interface at a second obtuse angle which is larger than the first angle.

2. (Original) A bipolar transistor as set forth in claim 1 wherein the minimum lateral extent (d) of the spacer (8) at the interface to the inner base portion (4a) is between 5 and 80 nm.

3. (Original) A bipolar transistor as set forth in claim 1 wherein the minimum lateral extent (d) of the spacer (8) at the interface to the inner base portion (4a) is between 10 and 60 nm.

4. (Original) A bipolar transistor as set forth in claim 1 wherein the minimum lateral extent (d) of the spacer (8) at the interface to the inner base portion (4a) is between 15 and 50 nm.
5. (Original) A bipolar transistor as set forth in claim 1 wherein the obtuse angle (α) between 100° and 135° .
6. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the second obtuse angle is $180^\circ - \beta$, wherein β is between 40° and 75° .
7. (Currently amended) A bipolar transistor as set forth in claim 1 with a higher dopant concentration in the outer base portion than in the inner base portion.
8. (Original) A bipolar transistor as set forth in claim 7 wherein the second base layer (12) or both base layers in the outer base portion (4b) have a dopant concentration which is increased in comparison with the inner base portion (4a), wherein the higher dopant concentration is restricted to a heightwise portion above a maximum of the dopant concentration in the inner base portion (4a).
9. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the inner base portion or the outer base portion or both base portions are additionally doped with carbon.
10. (Original) A bipolar transistor as set forth in claim 9 wherein the carbon concentration is between $5 \times 10^{18} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$.
11. (Original) A bipolar transistor as set forth in claim 10 wherein the carbon concentration is between $1 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{20} \text{ cm}^{-3}$.
12. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the second base layer (12) has a dopant concentration between $2 \times 10^{19} \text{ cm}^{-3}$ and $2 \times 10^{20} \text{ cm}^{-3}$.

13. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the first base layer (4) or the second base layer (12) or both contain a silicon-germanium alloy.

14. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the outer base portion (12) laterally only partially surrounds the emitter (9).

15. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the portion of the emitter which corresponds to the horizontal bar of the T-shape is separated by a second spacer in the form of an insulating layer from the subjacent outer base portion.

16. (Original) A bipolar transistor as set forth in claim 15 wherein the lateral ends of the portion of the emitter which corresponds to the horizontal bar of the T-shape is separated by a third spacer of insulating material from the outer base portion laterally adjoining same therebeneath.

17. (Currently amended) A bipolar transistor as set forth in claim 1 wherein the insulating material of the spacer (8) is SiO₂.

18. (Currently amended) A process for the production of a bipolar transistor as set forth in claim 1, comprising the steps:
depositing a layer stack on an epitaxial base layer which contains at least one auxiliary layer (5) to be later removed and a first insulating layer (6),
opening the emitter window by portion-wise removal of the layer stack,
depositing a second insulating layer (7), and
structuring the second insulating layer (7) in such a way that a spacer (8) of insulating material is produced at the edge of the emitter window, the lateral extent (d) of the spacer increasing from its interface with respect to the epitaxial base layer (4) with increasing height over the epitaxial base layer (4),
depositing an emitter layer (9) in the emitter window and on the second insulating layer (7) and producing an emitter of T-shaped cross-sectional profile by lateral structuring of the emitter layer and producing spacers (11) of insulating material at the side surfaces of the emitter,

exposing the semiconductor surface of the base layer (4) in the lateral regions of the outer base portion (4b) and depositing a raised base connection layer on said areas,

wherein the last three steps are carried out in such a way that a first interface formed by the emitter (9) and the spacer (8) meets a second interface formed by the emitter and the inner base portion at a first angle (α) which is either a right angle or an obtuse angle, and

a third interface formed by the spacer (8) and the raised base connection layer in the outer base portion (4b) meets a second interface formed by the spacer and the inner base portion at a second obtuse angle which is larger than the first angle.

19. (Currently amended) A process as set forth in claim 18 comprising the following steps for producing the emitter window:

providing a prepared substrate (1) on which at least one active bipolar transistor region and optionally additionally at least one active CMOS region is defined,

depositing an auxiliary layer (3) on the prepared substrate (1) and opening a window in the auxiliary layer (3) over the active bipolar transistor region, and

depositing an epitaxial base layer (4) into which base doping is introduced in situ.

20. (Currently amended) A process for the production of a bipolar transistor as set forth in claim 1 comprising the steps:

providing a prepared substrate on which either exclusively active bipolar transistor regions or both active bipolar transistor regions and also active CMOS regions are defined,

depositing an auxiliary layer (3) on the prepared substrate and opening windows in said auxiliary layer in the active bipolar transistor regions,

depositing an epitaxial base layer (4),

depositing an insulating layer (20) on the epitaxial base layer and producing an emitter window by portion-wise removal of the insulating layer (20),

depositing an emitter layer (9) and lateral structuring of the emitter in such a way that the emitter acquires a T-shaped cross-sectional profile, producing spacers (22) of insulating material at the side surfaces of the emitter,

selectively epitaxially depositing a raised base connection layer (23) on the exposed regions of the epitaxial base layer (4) forming a facet which meets the surface of the epitaxial base layer at an obtuse angle ($180^\circ - \beta$), and producing a spacer of insulating material which covers the facet.

21. (Currently amended) A process as set forth in claim 18 comprising the following steps after deposit of the raised base connection layer (12, 23):

removing the epitaxial base layer (4), the raised base connection layer (12) and the auxiliary layer (3) from collector connection regions of the bipolar transistors and optionally from the CMOS regions,

optionally implanting source, drain and gate regions to form MOS transistors and healing implantation damage, and

effecting a metallisation process for the bipolar and optionally at the same time also for the CMOS regions.

22. (Currently amended) A process as set forth in claim 18 wherein the epitaxial base layer (4) is produced by means of a differential epitaxy process in such a way that a monocrystalline layer is produced on the active bipolar transistor region and a polycrystalline layer is produced on insulating regions.

23. (Currently amended) A process as set forth in claim 18 wherein the second base layer (12) is selectively deposited by means of a selective epitaxy process on exposed regions of the first base layer (4).

24. (Currently amended) A process as set forth in claim 18 wherein the second base layer (12) is monocrystallinely deposited in regions adjoining the spacers (8).

26. (Currently amended) A process as set forth in claim 18 wherein the second base layer (12) is provided during the deposit operation in situ with a doping which is of the same conductivity type as the doping of the inner base.

27. (New) A process as set forth in claim 20 comprising the following steps after deposit of the raised base connection layer (12, 23):

removing the epitaxial base layer (4), the raised base connection layer (12) and the auxiliary layer (3) from collector connection regions of the bipolar transistors and optionally from the CMOS regions,

optionally implanting source, drain and gate regions to form MOS transistors and healing implantation damage, and

effecting a metallisation process for the bipolar and optionally at the same time also for the CMOS regions.